Amendments to the Specification

Please add the following new paragraph after the title on page 1:

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation of Application Serial No. 10/017,414, filed December 18, 2001, which is hereby incorporated herein by reference in its entirety for all purposes.

Please replace the paragraph beginning on page 6, line 2 with the following amended paragraph:

The NMOS transistors 41, 43, 45, 47, and 49, and the PMOS transistors 31 and 33 are connected between an input terminal Vin and an output termimal Vout in series. An input voltage is applied to the input terminal Vin. The output terminal Vout outputs a boosted voltage. The PMOS transistors 31 and 33 are positioned on the output terminal side as gate circuits. A substrate voltage of each NMOS is set to a reference voltage, i.e., a ground voltage according to the present embodiment. Each substrate voltage of ~~NMOS~~ PMOS transistors 31 and 33 is set to the boosted voltage ~~outputting~~ output from the output terminal Vout.

Please replace the paragraph beginning on page 6, line 13 with the following amended paragraph:

The PMOS transistors 51, 53, 55, 57, and 59 are connected to the corresponding NMOS transistors 41, 43, 45, 47, and 49, respectively, in parallel with each other. The substrate voltage of each ~~NMOS~~ PMOS transistor 51, 53, 55, 57 and 59 is also set to the boosted voltage ~~outputting~~ output from the output terminal Vout.

Please replace the paragraph beginning on page 6, line 19 with the following amended paragraph:

Each of level shift circuits 11 and 21 shifts a voltage level on a high voltage side of each of driving signals T1 and T2 transmitted between a source voltage level (or internal source voltage level) and a ground voltage level, from the voltage level (or internal voltage level) to the boosted voltage level. The driving signals T1 and [[T]] T2 slightly have a time when voltage levels are the same in the present embodiment, however, these signals are signals which have a complementary voltage level.

Please replace the paragraph beginning on page 12, line 2 with the following amended paragraph:

Next, when the voltage generation signals S1 and S2 are L levels, the driving signal T1 is the H level, and the driving signal [[T]] T2 is the L level, the input voltage is supplied to the terminal for the VS1. The NMOS 41 and the PMOS 51 become in the

non-conductive state and the PMOS 33 becomes in the conductive state. Since the input voltage is maintained in one electrode of the capacitor and the input voltage is supplied to the other electrode, the capacitor is started to be discharged. Thereby, a voltage is boosted for a charge in which a voltage on one electrode side is stoked. If the stocked charge corresponds to the input voltage, the input voltage is boosted double. The boosted voltage is supplied to the output terminal Vout electrically connected to the terminal VC6. By this way, a voltage in which the input voltage is boosted double can be obtained. The boosted voltage is stably maintained by repeating like this operation.

Please replace the paragraph beginning on page 17, line 6 with the following amended paragraph:

An output signal from the shift level circuit 111 and an output signal from the NOR gate [[103]] 13 are input to the NOR gate 103. The output signal of the NOR gate 103 is supplied to a gate electrode of the PMOS 153 and to a gate electrode of the NMOS 143 via an inverter 105.

Please replace the abstract with the following amended abstract:

~~According to the present invention, in a~~ A boost voltage circuit[[,]] includes a plurality of N channel ~~typed~~ type MOS transistors ~~are~~ connected between an input terminal and an output terminal in series, wherein ~~and~~ one electrode of each of the N channel ~~typed~~

type MOS ~~transistor~~ transistors is connected to each of external terminals ~~VC1 toVC5~~ to which a capacitor can be connected, to generate a boost voltage. ~~Each~~ A plurality of P channel ~~typed~~ type MOS transistors are respectively connected to each of the N channel type MOS transistors in parallel ~~in the boost voltage circuit with the above constitution~~. Thereby, ~~it is possible to provide~~ a boost voltage circuit with improved ~~to improve~~ stability ~~in staring~~ is provided so that the boost voltage circuit is started without increase of ~~the~~ consumption current.